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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/688,049 | 10/16/2003 | Farhood Moraveji | MIC-00002 | 9204 |

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BEVER HOFFMAN & HARMS, LLP
TRI-VALLEY OFFICE
1432 CONCANNON BLVD., BLDG. G
LIVERMORE, CA 94550

| EXAMINER | |
|---|---|
| CHOE, HENRY | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2817 | |

DATE MAILED: 01/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/688,049 | MORAVEJI, FARHOOD | |
| | Examiner | Art Unit | |
| | Henry K Choe | 2817 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,8,10,11,18,19 and 23* is/are rejected.

7)☒ Claim(s) *4-7,9,12-17,20-22 and 24-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 8, 18 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Rybicki (Fig. 2B).

Regarding claims 1 and 18, Rybicki (Fig. 2B) discloses an amplifier circuit comprising a first input terminal (S), a first output terminal (VOUT), a first complementary metal oxide semiconductor inverter (18, 24) which is coupled between the first input terminal (S) and the first output terminal (VOUT), and a first bias circuit (42, 12, 44, VAG) which applies linear biasing to an input (S) of the first CMOS inverter (18, 24) and wherein the first bias circuit (42, 12, 44, VAG) being coupled between an output (outputs of 18 and 24) of the first CMOS inverter (18, 24) and the input (S) of the first CMOS inverter (18, 24).

Regarding claims 8 and 23, Rybicki (Fig. 2B) discloses an amplifier circuit comprising a CMOS inverter (18, 24) coupled between an upper supply voltage (VDD) and a lower supply voltage (VSS), and an operational amplifier (12, 44, VAG) including a non-inverting input (+input of 12) coupled to an output (VOUT) of the CMOS inverter (18, 24) and an inverting input (- input of 12) coupled to receive a reference voltage

(VAG) and an output (output of 12) coupled to an input (a node between 12 and 20) of the CMOS inverter (18, 24).

Claims 1-3, 10, 11, 18 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Leuthold (Fig. 2).

Regarding claims 1, 10, 11 and 18, Leuthold (Fig. 2) discloses an amplifier circuit comprising a first input terminal (UE), a first output terminal (UR), a first complementary metal oxide semiconductor inverter (P, N) which is coupled between the first input terminal (UE) and the first output terminal (UR), and a resistor R can be read as the claimed a first bias circuit since the resistor R affects the bias voltage of the inverter P and N and the first bias circuit R applies linear biasing to an input (input of P and N) of the first CMOS inverter (P, N) and wherein the first bias circuit (R) being coupled between an output (drain terminals of P and N) of the first CMOS inverter (P, N) and the input (gates of P and N) of the first CMOS inverter (P, N).

Regarding claim 2, the first input terminal (UE) is coupled to the input (gate terminals of P and N) of the first CMOS inverter (P, N) by a first capacitor (C1), and wherein the first output terminal (UR) is coupled to the output (drain terminals of P and N) of the first CMOS inverter (P, N) by a second capacitor (C2).

Regarding claims 3 and 19, the first CMOS inverter (P, N) includes a p-type MOS transistor (P), an n-type MOS transistor (N), wherein the PMOS transistor (P) and the NMOS transistor (N) are serially connected between an upper supply voltage (+V) and a lower supply voltage (ground), wherein a gate (upper G) of the PMOS transistor (P) and a gate (lower G) of the NMOS transistor (N) are connected to the input (a node between

C1 and R) of the first CMOS inverter (P, N), and wherein a drain (upper D) of the PMOS transistor (P) and a drain (lower D) of the NMOS transistor (N) are connected to the output (a node between upper D and lower D) of the first CMOS inverter (P,N).

### *Allowable Subject Matter*

Claims 4-7, 9, 12-17, 20-22 and 24-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patent numbers (5,777,516; 6,433,637; 6,836,186; 4,241,313) are the inverter circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry Choe whose telephone number is (571) 272-1760.

HENRY CHOE
PRIMARY EXAMINER

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